CLAIMS

What is claimed is:

1. A method comprising:

executing a speculative read-reordered load instruction;

storing memory conflict information representing the speculative read-reordered load;

matching an address of a potentially conflicting load against an address of the stored memory conflict information; and

invalidating stored memory conflict information with a matching address.

2. The method of claim 1, wherein the stored memory conflict information is invalidated if the stored memory conflict information has a different value than the potentially conflicting load.

3. The method of claim 2, further comprising executing a read re-ordered load check instruction to determine the validity of the speculative read re-ordered load.

4. The method of claim 1, wherein the memory conflict information is stored in a read re-ordered load address table (RRLAT).

5. The method of claim 5, further comprising updating the stored memory conflict information by setting a validity bit in the RRLAT to a valid state when new memory conflict information is stored.

6. The method of claim 6, further comprising setting the validity bit to an invalid state if a later conflicting load operation is executed.

7. A processor, comprising:

a RRLAT to store memory conflict information representing a speculative read re-ordered load; and

a monitor to compare a potentially conflicting load against the stored memory conflict information.

8. The processor of claim 8, wherein the stored memory conflict information is invalidated if the stored memory conflict has a matching address.

9. The processor of claim 8, wherein the stored memory conflict information is invalidated if the stored memory conflict has a matching address and a different value than the potentially conflicting load.

10. The processor of claim 10, wherein the RRLAT is referenced upon the execution of a read re-ordered load check instruction to determine the validity of the speculative read re-ordered load.

11. The processor of claim 8, wherein the RRLAT may be any one of a direct-mapped, multi-way set associative, and fully associative data structure.

12. The processor of claim 8, wherein the RRLAT is portioned among hardware thread contexts.

13. The processor of claim 8, wherein the RRLAT includes storage locations for an address, a target register ID, a value, and validity information associated with the speculative read re-ordered load.

14. A computer system, comprising:

a processor, including:

a RRLAT to store memory conflict information representing a speculative read re-ordered load;

a monitor to compare a potentially conflicting load against the stored memory conflict information, and to invalidate the stored memory conflict information if the stored memory conflict information has a matching address and a different value than the potentially conflicting load; and

a cache memory.

15. The computer system of claim 16, wherein the monitor unit executes a read re-ordered load check instruction to determine the validity of the speculative read re-ordered load.

16. A computer system, comprising:

a first processor; and

a second processor, including:

a RRLAT to store memory conflict information representing a speculative read re-ordered load received from the second processor; and

a monitor to compare a potentially conflicting load received

from the first processor against the stored memory conflict information, and to invalidate the stored memory conflict information if the stored memory conflict information has a matching address and a different value than the potentially conflicting load.

17. The computer system of claim 19, wherein the monitor unit executes a read re-ordered load check instruction to determine the validity of the speculative read re-ordered load.

18. A computer system, comprising:

a processor, including:

a RRLAT to store memory conflict information representing a speculative read re-ordered load;

a monitor to compare a potentially conflicting load against the stored memory conflict information, and to invalidate the stored memory conflict information if the stored memory conflict information has a matching address and a different value than the potentially conflicting load; and

a cache memory; and

a memory device coupled to the processor.

19. The computer system of claim 21, wherein the monitor unit validates stored memory conflict information with a matching address if the stored memory conflict information has a matching value to the potentially conflicting load.

20. The computer system of claim 22, wherein the monitor unit executes a read re-ordered load check instruction to test the validity of the speculative read re-ordered load.

21. The computer system of claim 21, further comprising a bus to control communications between the processor and the memory device.

22. A machine-readable medium storing a sequence of instructions that, when executed by a machine, cause the machine to:

execute a speculative read-reordered load instruction;

store memory conflict information representing the speculative read-reordered load;

match the address of a potentially conflicting load against the address of the stored memory conflict information; and

invalidate stored memory conflict information with a matching address if the stored memory conflict information has a different value than the potentially conflicting load.

23. The machine-readable medium of claim 25, the sequence of instructions, when executed by the computer system, further causing the computer system to validate stored memory conflict information with a matching address if the stored memory conflict information has a matching value to the potentially conflicting load.

24. The machine-readable medium of claim 26, the sequence of instructions, when executed by the computer system, further causing the computer system to execute a read re-ordered load check instruction to determine the validity of the speculative read re-ordered load.